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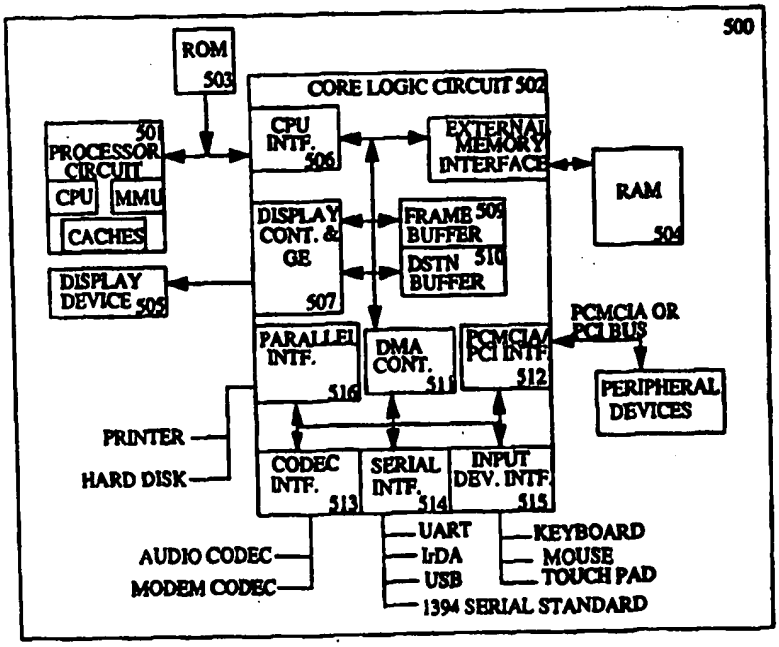
(54) Title: HIGH PERFORMANCE, HIGHLY INTEGRATED COMPUTER ARCHITECTURE WITH EXTENDIBLE EMBEDDED MEMORY

(57) Abstract

A high performance computer system architecture that is highly integrated and extendible is presented. The computer system architecture comprises an integrated processor circuit, a core logic circuit incorporates at least a display controller. The embedded memory may be partitioned into multiple buffers or may consist of separate and independent buffers. The ROM is connected to a bus between the integrated processor circuit and the core logic circuit. The RAM is connected to the core logic circuit. The central processor may also be intergrated with the core logic circuit.



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HIGH PERFORMANCE, HIGHLY INTEGRATED COMPUTER ARCHITECTURE WITH EXTENDIBLE EMBEDDED MEMORY

FIELD OF THE INVENTION

The invention generally relates to computer systems, and more particularly relates to computer system architecture.

BACKGROUND OF THE INVENTION

With the advances of semiconductor and computer technology, computer systems are becoming faster and at the same time smaller in size. Desk-top and even lap-top computer systems now possess processing speeds of main-frame computers that used to fill up a small room. Even hand-held computer systems such as personal digital assistants (PDA), which are becoming more popular, are getting more powerful. As computer systems become more miniaturized and inexpensive, more demands are constantly being required of them as well. For instance, they are being asked to perform more time-consuming and complex tasks involving graphics and video processing.

Computer graphics and video processing generally require heavy data transfer. A graphic or video image is made up of large blocks of pixels which translate into even larger blocks of data bytes. After graphics and video images enter a computer system through video ports, network ports, or mass storage devices such as CD-ROMS, they are stored in a system/main memory. Graphic and video images are then transferred to the graphics/video controller, where image processing is performed. After processing, however, graphics and video image data are transferred back to system/main memory for storage before these images are displayed.

In general, graphics and video image data for a display screen are stored as a bitmap in the system memory which promotes ease and efficient display device download. In other words, the system memory is used to hold a bit-per-bit representation of what is being displayed on the monitor. With the resolution and details of graphics and video images

constantly improving, the number of bytes/words and hence, the sizes of graphics and video image bitmaps are getting larger. As a result, a large system memory is often required.

At the same time, as computer systems become more powerful and more miniaturized, power-conservation also presents a difficult challenge to overcome. Because of their small size, hand-held computer systems are powered by battery which have limited operating duration. Since more power is required for faster and more powerful processors, innovative solutions are required to conserve power and thereby extend the battery operating duration.

For the above reasons, it is an on-going battle to come up with innovative computer system architectures with improved system performance as well as improved power-conservation. Referring now to Figure 1 illustrating a Prior Art computer system architecture. As shown in Figure 1, Prior Art computer system architecture 100 is a highly integrated system which consists of integrated processor circuit 101, peripheral controller 102, read-only-memory (ROM) 103, and random access memory (RAM) 104. The highly integrated architecture allows power to be conserved. Prior Art computer system architecture 100 may also include a peripheral controller if there is a need to interface with complex and/or high pin-count peripherals that are not provided in integrated processor circuit 101.

While peripheral controller 102 is connected to integrated processor circuit 101 on one end, ROM 103 and RAM 104 are connected to integrated processor circuit 101 on the opposite end. Integrated processor circuit 101 comprises a processing unit 105, memory interface 106, display controller 107, direct memory access (DMA) controller 108, and core logic functions including encoder/decoder (CODEC) interface 109, parallel interface 110, serial interface 111, and input device interface 112. Processing unit 105 integrates a central processing unit (CPU), a memory management unit (MMU), together with instruction/data caches.

CODEC interface 109 provides the interface for an audio source and/or modem to connect to integrated processor circuit 101. Parallel interface 110 allows parallel input/output (I/O) devices such as hard disks, printers, etc. to connect to integrated processor circuit 101. Serial interface 111 provides the interface for serial I/O devices such as universal asynchronous receiver transmitter (UART) to connect to integrated processor circuit 101. Input device interface 112 provides the interface for input devices such as keyboard, mouse, and touch pad to connect to integrated processor circuit 101.

DMA controller 108 accesses data stored in RAM 104 via memory interface 106 and provides the data to peripheral devices connected to CODEC interface 109, parallel interface 110, serial interface 111, or input device interface 112. Display controller 107 request and accesses the video/graphics data from RAM 104 via memory interface 106. Display controller 107 then formats and sends the formatted data to a display device such as a liquid crystal display (LCD), a cathode ray tube (CRT), or a television (TV) monitor.

In Prior Art computer system architecture 100, a single memory bus is used to connect integrated processor circuit 101 to ROM 103 and RAM 104. As such, only one memory (i.e., either ROM 103 or RAM 104) can be accessed at any one time. Moreover, because RAM 104 is a unified memory shared between the CPU, display controller 108, and peripheral devices, the memory bandwidth is extremely limited and is therefore a bottleneck. As a result, the above Prior Art architecture is only adequate for low performance applications. The capability to perform processor and memory intensive tasks such as software modem, graphics processing and display, or video display is extremely limited if not impossible under this architecture.

Figure 2 illustrates another Prior Art computer system architecture that offers slightly improved performance over the architecture described in Figure 1 above. As shown in Figure 2, Prior Art computer system architecture 200 consists of an

integrated processor circuit 201, core logic & display controller 202, ROM 203, and RAM 204.

Integrated processor circuit 201 integrates a CPU, an MMU, together with instruction/data caches. Core logic & display controller 202 performs core logic function interfaces including parallel I/O interface, serial I/O interface, input device interface, and audio device interface. Additionally, core logic & display controller 202 performs graphics and video data accesses as well as data formatting for a display device.

In Prior Art computer system architecture 200, ROM 203 is connected to a bus between integrated processor circuit 201 and core logic & display controller 202. In so doing, direct and fast access to ROM 203 by integrated processor circuit 201 or core logic & display controller 202 for stored instructions and data is possible. However, RAM 204 is a unified memory shared by integrated processor circuit 201, core logic & display controller 202, and peripheral devices. As such, in accessing RAM 204, the same memory bandwidth limitation and bottleneck problems still remain. Moreover, because core logic & display controller 202 is between integrated processor circuit 201 and RAM 204, while access of display data by the integrated display controller inside core logic & display controller 202 is direct and fast, any effort to access data stored in RAM 204 by integrated processor circuit 201 is subject to further delay.

Figure 3 illustrates a Prior Art computer system architecture that is more suitable for high end and high performance systems such as Internet televisions (Internet TV), high end network computers, etc. As shown in Figure 3, Prior Art computer system architecture 300 consists of an integrated processor circuit 301, core logic 302, display controller 303, ROM 304, RAM 305, and frame buffer 306. Prior Art computer system architecture 300 may further include additional peripherals which like display controller 303 are normally connected to a peripheral bus such as an (ISA) bus or a peripheral computer interconnection (PCI) bus.

Integrated processor circuit 301 integrates a CPU, an MMU, together with instruction/data caches. Core logic 302 performs core logic function interfaces including parallel I/O interface, serial I/O interface, input device interface, and audio device interface. In this Prior Art architecture, display controller 304 is separate from core logic 302.

In Prior Art computer system architecture 300, ROM 304 is connected to a bus between integrated processor circuit 301 and core logic 302. In so doing, although there is still contention between integrated processor circuit 301 and core logic 302, direct and fast access to ROM 304 for the stored instructions is possible. RAM 305 is separate from frame buffer 306 which is specifically used to store display data for display controller 303. As such, in accessing RAM 305, the memory bandwidth limitation and bottleneck problem are greatly alleviated. However, since ROM 304 and RAM 305 are still shared by integrated processor circuit 301 and core logic 302, contention is still a problem. Adding external frame buffer 306 in this architecture translates to added costs as well as decreased power conservation due to added pin count. Accordingly, despite its high performance capability, the architecture of Figure 3 may not be suitable for portable or hand held computer systems due its size and costs.

Figure 4 illustrates yet another Prior Art computer system architecture. As shown in Figure 4, Prior Art computer system architecture 400 consists of a main processor circuit 401, an auxiliary processor circuit 402, system ROM 403, system RAM 404, and frame buffer 405.

Main processor circuit 401 integrates a CPU, a MMU, instruction/data caches, a memory interface, a DMA controller, a CODEC interface, a serial interface, and an input device interface. The memory interface of main processor circuit 401 controls access to the system bus to which main processor circuit 401, auxiliary processor circuit 402, ROM 403, and RAM 404 are connected. Auxiliary processor circuit 402 also integrates a CPU and memory interface, and a DMA controller.

Auxiliary processor circuit 402 further integrates a display controller, a serial port interface, a personal computers memory card international association (PCMCIA) interface, an IrDA, and other device interfaces. Frame buffer 405 is provided separately for the display controller over a display bus. Accordingly, display tasks such as display refresh function does not consume system RAM 403 bandwidth. However, an external frame buffer requires additional pin count which translates to added costs and increased power consumption. Furthermore, in the event main processor circuit 401 wants to access frame buffer 405, two levels of arbitration are required which means added delays.

Since one system bus is used for both system RAM 403 and system ROM 404, either RAM 403 or ROM 404 (but not both) can be accessed at any given time. This places a significant access restriction on both main processor circuit 401 and auxiliary processor circuit 402 which causes a reduction in overall system performance. Additionally, any DMA transfer is required to go through the memory interfaces which control system bus access. As such, a penalty of time is required for the bus arbitration. Furthermore, a rather complex DMA access priority scheme is needed to arbitrate when several devices are contending for control of the system bus.

Thus, a need exists for a high performance, cost effective, power efficient, and extendible computer system architecture for portable and hand-held computer systems.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides a high performance, cost effective, power efficient, and extendible computer system architecture for portable and hand-held computer systems.

The present invention meets the above need with an embodiment of a computer system that comprises: a central processor, an integrated core logic circuit, a read only memory (ROM), and a random access memory (RAM). The integrated core

logic circuit is coupled to the central processor. The ROM is coupled to the central processor and the integrated core logic circuit. The RAM is coupled to the integrated core logic circuit.

The integrated core logic circuit comprises a display controller and extendible embedded memory. In one embodiment, the embedded memory can be partitioned into N buffers wherein the N buffers include a frame buffer and a dual-scan super twisted neumatic (DSTN) buffer. In another embodiment, the embedded memory comprises N separate buffers.

In an alternate embodiment of the computer system architecture in accordance to the present invention, the central processor is integrated with the core logic circuit to achieve a highly integrated computer system architecture. The alternate embodiment also has an extendible embedded memory much like the first embodiment.

All the features and advantages of the present invention will become apparent from the following detailed description of its preferred embodiment whose description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Prior Art Figure 1 is a block diagram illustrating a Prior Art computer system architecture.

Prior Art Figure 2 is a block diagram illustrating another Prior Art computer system architecture.

Prior Art Figure 3 is a block diagram illustrating a high performance Prior Art computer system architecture

Prior Art Figure 4 is a block diagram illustrating yet another Prior Art computer system architecture

Figure 5 is a block diagram illustrating an embodiment of the computer system architecture in accordance to the present invention.

Figure 6 is a block diagram illustrating an alternate embodiment of the computer system architecture in accordance to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Figure 5 illustrates an embodiment of the computer system architecture in accordance to the present invention. As shown in Figure 5, computer system architecture 500 consists of integrated processor circuit 501, core logic circuit 502, ROM 503, RAM 504, and display device 505 such as an LCD. Computer system architecture 500 may further include additional peripherals which are normally connected to a peripheral bus such as a peripheral computer (PCMCIA) or a peripheral computer interconnection (PCI) bus. ROM 503 is connected to a bus between integrated processor circuit 501 and core logic circuit 502. RAM 504 is connected to core logic circuit 502. Accordingly, access from the CPU must go through core logic circuit 502.

Integrated processor circuit 501 integrates a CPU, an MMU, together with instruction/data caches. The MMU arbitrates data access requests and controls instruction/data transfers between ROM 503, RAM 504, and instruction/data caches for executing and processing by the CPU.

Core logic circuit 502 comprises CPU interface 506, display controller & graphics engine 507, memory interface 508, frame buffer 509, dual scan super twisted neumatic (DSTN) display buffer 510, DMA controller 511, PCMCIA or PCI interface 512, CODEC interface 513, serial interface 514, input device interface 515, and parallel interface 516. Data can be transferred between various peripheral devices and frame buffer 509 and DSTN buffer 510 using DMA controller 511. Because core logic circuit 502 does not have an integrated microprocessor,

core logic circuit 502 does not have to access ROM 503 for stored instructions. Accordingly, integrated processor circuit 501 does not have to contend for accessing ROM 503 which improves performance.

CPU interface 506 receives requests from integrated processor circuit 501 to access frame buffer 509 and DSTN buffer 510. Additionally, CPU interface 506 relays the request to access RAM 504 from integrated processor circuit 501 to memory interface 508 for arbitration. Memory interface 508 performs data transfers to/from RAM 504. Hence, there is only one level of arbitration for the CPU to access RAM 504 which again improves performance. Display controller & graphics engine 507 performs graphics and video data accesses such as display refresh access, hardware cursor access, graphics engine access, and half frame buffer access. Moreover, display controller & graphics engine 507 performs other tasks such as data processing, rendering, and formatting for display device 505. Frame buffer 509 and DSTN buffer 510 temporarily store the processed data prior to being sent to display device 505 by display controller & graphics engine 507.

PCMCIA or PCI interface 512 provides the interface for a PCMCIA or a PCI bus to connect to core logic circuit 502. CODEC interface 513 provides the interface for an audio source and/or modem to connect to core logic circuit 502. Serial interface 514 allows serial input/output (I/O) devices such as universal asynchronous receiver transmitter (UART), infrared (IrDA), universal serial bus (USB), IEEE serial communications standard 1394, etc. to connect to core logic circuit 502. Input device interface 515 provides the interface for input devices such as keyboard, mouse, touch pad to connect to core logic circuit 502. Parallel interface 516 provides the interface for parallel devices such as printers and hard disk drives to connect to core logic circuit 502.

DMA controller 511 accesses data stored in RAM 504 via memory interface 508 and subsequently transfers the data retrieved to frame buffer 509, DSTN buffer 510, PCMCIA or PCI

interface 512, CODEC interface 513, serial interface 514, and input device interface 515. These interfaces in turn provide the data to the peripheral devices connected to them. DMA controller 511 also transfers data from frame buffer 509, DSTN buffer 510, and the peripheral devices to RAM 504. Because access to RAM 504 is controlled by CPU interface 506 and memory interface 508, respectively, which both reside inside core logic circuit 502, there is only one memory arbitration unit. Accordingly, the DMA accessing scheme is rather easy to implement.

ROM 503, which is used to store instructions, is connected between integrated processor circuit 501 and core logic circuit 502. In so doing, direct and fast access to ROM 503 for the stored instructions is possible. Moreover, integrated processor circuit 501 normally does not have to contend for access to ROM 503 because core logic circuit 502 does not have an integrated microprocessor to execute the instructions stored in ROM 503.

In the present invention, RAM 504 is separate from the frame buffer. There are two separate buffers: frame buffer 509 and DSTN buffer 510 in the present computer architecture. Having separate frame buffer 509 and DSTN buffer 510 allows, for example, incoming video images to be stored into frame buffer 509 without affecting the display performance.

Because frame buffer 509 and DSTN buffer 510 are separate from RAM 504, in accessing RAM 504, the memory bandwidth limitation and bottleneck problem are greatly alleviated given that video and graphics tasks involve heavy data transfer. Moreover, the present invention allows access to ROM 503 and RAM 504 simultaneously by integrated processor circuit 501 and core logic 502. Also, the bus connecting RAM 504 to core logic circuit 502 can operate asynchronously to the bus connecting ROM 503 to integrated processor circuit 501 which is an advantage since the speed of RAM 504 may be more than ROM 503.

Moreover, both frame buffer 509 and DSTN buffer 510 are embedded memories internally to core logic circuit 502 which

allows a wider interface (e.g., 64-bit, 128-bit, etc.) than external memories which normally only have 32-bit interface for economic reasons (e.g., reduced pin count). As a result, the average latency for memory access is reduced and higher resolution displays and color depth are allowed. It is to be appreciated that both frame buffer 509 and DSTN buffer 510 can also be accessed by the CPU of integrated processor circuit 501 thereby the internal memories are fully utilized.

In the preferred embodiment, frame buffer 509 and DSTN buffer 510 are implemented by dividing a common embedded memory into two. In essence, the common embedded memory is extendible to accommodate additional memory bandwidth requirements. In implementing this extendible embedded memory, a predetermined range of memory addresses is reserved for frame buffer 509 and a different range of memory addresses is reserved for DSTN buffer 510. Moreover, the common memory incorporates two memory ports, two address buses, and two data buses. The boundary between buffer 509 and DSTN buffer 510 can be arbitrary. It is to be appreciated that the common embedded memory may be divided into more than two buffers as in the preferred embodiment depending on the needs. For example, local area network (LAN) and wide area network (WAN) functions may be integrated into core logic circuit 502 which then requires a data buffer management with a large data buffer. In which case, the common embedded memory is divided into three portions. However, it is to be appreciated that embedded frame buffer 509 and DSTN buffer 510 can also be two separate and independent memories and still be within the scope of the invention.

In having an embedded memory, which is divided into multiple memory modules such as frame buffer 509 and DSTN buffer 510, inside core logic circuit 502, the computer system architecture of the present invention can easily be extended by subdividing/partitioning the embedded memory into sub-modules to accommodate the ever growing memory bandwidth demands placed on the computer systems without a substantial

degradation of performance.

As discussed, the computer system architecture of the present invention is highly integrated (e.g., having an integrated processor circuit and an integrated core logic circuit with embedded memory). As a result, the pin-count is greatly reduced which coupled with embedded memory translates to increased performance and reduced power consumption. Moreover, the integrated architecture with embedded memory of the present invention means that the computer system is quite cost effective.

Reference is now made to Figure 6 illustrating an alternate embodiment of the computer system architecture in accordance to the present invention. As shown in Figure 6, the computer system architecture 600 consists of an integrated processor & core logic circuit 601, ROM 602, RAM 603, and display device 604 such as an LCD or a cathode ray tube (CRT). Computer system architecture 600 may further include additional peripherals such as a PCMCIA interface or a PCI interface. ROM 602 and RAM 603 is connected to integrated processor and core logic circuit 601.

Integrated processor & core logic circuit 601 integrates a CPU, an MMU, instruction/data caches, and core logic circuit. The MMU arbitrates data access requests and controls instruction/data transfers between ROM 602, RAM 603, and instruction/data caches for executing and processing by the CPU.

The integrated core logic circuit inside integrated processor & core logic circuit 601 comprises display controller & graphics engine 605, external memory interface 606, frame buffer 607, DSTN buffer 608, DMA controller 609, PCMCIA or PCI interface 610, CODEC interface 611, serial interface 612, parallel interface 613, and input device interface 614.

Memory interface 606 performs arbitration and data accesses to/from ROM 602 and RAM 603. Hence, there is only one level of arbitration for the CPU to access RAM 603 which again improves performance. Display controller & graphics engine 605

performs graphics and video data accesses such as display refresh access, hardware cursor access, graphics engine access, and DSTN half frame buffer access. Moreover, display controller & graphics engine 605 performs other tasks such as data processing, rendering, and formatting for display device 604. Frame buffer 607 and DSTN buffer 608 temporarily store the processed data prior to being sent to display device 604 by display controller & graphics engine 605.

PCMCIA or PCI interface 610 provides the interface for a PCMCIA or a PCI bus to connect to integrated processor & core logic circuit 601. CODEC interface 611 provides the interface for an audio source and/or modem to connect to integrated processor & core logic circuit 601. Serial interface 612 allows serial input/output (I/O) devices such as universal asynchronous receiver transmitter (UART), infrared sensor (IrDA), universal serial bus (USB), IEEE serial communications standard 1394, etc. to connect to integrated processor & core logic circuit 601. Parallel interface 613 allows parallel I/O devices such as printers and hard disk drives to connect to integrated processor & core logic circuit 601. Input device interface 614 provides the interface for input devices such as keyboard, mouse, touch pad to connect integrated processor & core logic circuit 601.

DMA controller 609 accesses data stored in RAM 603 via memory interface 606 and subsequently transfers the data retrieved to frame buffer 607, DSTN buffer 608, PCMCIA or PCI interface 610, CODEC interface 611, serial interface 612, parallel interface 613, and input device interface 614. These interfaces in turn provide the data to the peripheral devices connected to them. DMA controller 609 also transfers data from frame buffer 607, DSTN buffer 608, and the peripheral devices to RAM 603. DMA controller 609 also transfers data to/from peripheral devices from/to frame buffer 607 or DSTN buffer 608. Because accesses to both ROM 602 and RAM 603 are controlled by memory interface 606, which resides inside integrated processor & core logic circuit 601, there is only one memory arbitration

unit. Accordingly, the DMA accessing scheme is rather easy to implement.

ROM 602 is connected to integrated processor & core logic circuit 601. In the alternate embodiment, RAM 603 is separate from the frame buffer. There are two separate buffers: frame buffer 607 and DSTN buffer 608 in the present computer architecture. Having separate frame buffer 607 and DSTN buffer 608 allows access to, for example, incoming data from a peripheral device stored in frame buffer 607 or DSTN buffer 608 without adversely affecting the display controller 605 performance.

Because frame buffer 607 and DSTN buffer 608 are separate from RAM 603, in accessing RAM 603, the memory bandwidth limitation and bottleneck problem are greatly alleviated given that video and graphics tasks involve heavy data transfer. Moreover, both frame buffer 607 and DSTN buffer 608 are embedded memories internally to integrated processor & core logic circuit 601 which allows a wider interface (e.g., 64-bit, 128-bit, etc.) than external memories which normally only has 32-bit interface for economic reasons (e.g., reduced pin count). As a result, the average latency for memory access is reduced and higher resolution display and color depth are allowed. It is to be appreciated that both frame buffer 607 and DSTN buffer 608 can also be accessed by the CPU of integrated processor & core logic circuit 601 thereby the internal memories are fully utilized.

In the preferred embodiment, frame buffer 607 and DSTN buffer 608 are implemented by dividing a common embedded memory into two. In essence, the common embedded memory is extendible to accommodate additional memory bandwidth requirements. In implementing this extendible embedded memory, a predetermined range of memory addresses is reserved for frame buffer 607 and a different range of memory addresses is reserved for DSTN buffer 608. Moreover, the common memory incorporates two memory ports, two address buses, and two data buses. The boundary between frame buffer 607 and DSTN buffer 608 can be

arbitrary. It is to be appreciated that the common embedded memory may be divided into more than two buffers as in the preferred embodiment depending on the needs. For example, local area network (LAN) and wide area network (WAN) functions may be integrated into integrated processor & core logic circuit 601 which then requires a data buffer management with a large data buffer. In which case, the common embedded memory is divided into three portions. However, it is to be appreciated that embedded frame buffer 607 and DSTN buffer 608 can also be two separate and independent memories and still be within the scope of the invention.

In having an embedded memory, which is divided into multiple memory modules such as frame buffer 607 and DSTN buffer 608, inside integrated processor & core logic circuit 601, the computer system architecture of the present invention can easily be extended by subdividing/partitioning the embedded memory into sub-modules to accommodate the ever growing memory bandwidth demands placed on the computer systems without a substantial degradation of performance.

As discussed, the computer system architecture of the present invention is highly integrated (e.g., having a CPU, MMU, instructions caches, and core logic functions integrated into an integrated processor & core logic circuit with embedded memory). As a result, the pin-count is greatly reduced which coupled with embedded memory translates to increased performance and reduced power consumption. Moreover, the integrated architecture with embedded memory of the present invention means that the computer system is quite cost effective.

It is to be appreciated that all of the processing and core logic components described above in the detailed descriptions of the two embodiments in accordance to the present invention such as processor circuit, display controller, graphics engine, frame buffer, DSTN buffer, DMA controller, CPU interface, external memory interface, PCI interface, PCMCIA interface, etc. are well-known to people of

ordinary skill in the art. Although each system designer may implement these components such that they may slightly be different and thereby provide slightly different functions, it is to be appreciated that their overall functions should remain substantially similar as they are well known in the art. Accordingly, for the sake of brevity and clarity, these components were not discussed in detail above. Rather, they are discussed rather briefly in order to emphasize the novelty of the computer system architecture under the present invention.

The embodiments of the present invention, two computer system architectures that have high performance capability, cost effective, extendible to accommodate increased memory bandwidth demands, and increased power conservation are thus described. While the present invention has been described in particular embodiments, the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

1. A computer system comprising:

a central processor;

an integrated core logic circuit coupled to the central processor, wherein the integrated core logic circuit comprising a display controller and extendible embedded memory;

a read only memory (ROM) coupled to the central processor and the integrated core logic circuit; and

a random access memory (RAM) coupled to the integrated core logic circuit.

2. The computer system of claim 1, wherein the embedded memory is partitioned into N buffers.

3. The computer system of claim 2, wherein the N buffers are a frame buffer and a dual scan twisted neumatic (DSTN) buffer.

4. The computer system of claim 1, wherein the embedded memory comprises N separate and independent buffers.

5. The computer system of claim 4, wherein the N buffers are a frame buffer and a DSTN buffer.

6. The computer system of claim 2, wherein the integrated core logic circuit further comprises a direct memory access (DMA) controller.

7. The computer system of claim 6, wherein the integrated core logic circuit further comprises a central processor interface and a memory interface, wherein the central processor and the ROM are coupled to the central processor interface and the RAM is coupled to the memory interface

8. The computer system of claim 7, wherein the integrated core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, a parallel interface, an input device interface, and a peripheral connect interface bus (PCI) interface.

9. The computer system of claim 7, wherein the integrated core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, an input device interface, and a personal computers memory card international association (PCMCIA) interface.

10. A computer system comprising:

an integrated central processing and core logic circuit comprising a central processor, a display controller and extendible embedded memory;

a read only memory (ROM) coupled to the integrated processing and core logic circuit; and

a random access memory (RAM) coupled to the integrated processing and core logic circuit.

11. The computer system of claim 10, wherein the embedded memory is partitioned into N buffers.

12. The computer system of claim 11, wherein the N buffers are a frame buffer and a DSTN buffer.

13. The computer system of claim 10, wherein the embedded memory comprises N separate and independent buffers.

14. The computer system of claim 13, wherein the N buffers are a frame buffer and a DSTN buffer.

15. The computer system of claim 11, wherein the integrated processing and core logic circuit further comprises a direct memory access (DMA) controller.

16. The computer system of claim 15, wherein the integrated processing and core logic circuit further comprises a memory interface, wherein the ROM and the RAM are coupled to the memory interface.

17. The computer system of claim 16, wherein the integrated processing and core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, a parallel interface, an input device interface, and a peripheral connect interface bus (PCI) interface.

18. The computer system of claim 16, wherein the integrated core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, an input device interface, and a PCMCIA interface.

19. An integrated core logic circuit comprising:

a display controller;

embedded memory coupled to the display controller, the embedded memory is partitioned into N buffers; and

a DMA controller coupled to the embedded memory.

20. The integrated core logic circuit of claim 19, wherein the N buffers comprising a frame buffer and a DSTN buffer.

21. The integrated core logic circuit of claim 20, wherein the core logic circuit further comprises a direct memory access (DMA) controller.

22. The integrated core logic circuit of claim 21, wherein the integrated core logic circuit further comprises a central processor interface and an external memory interface, wherein the central processor and the ROM are coupled to the central processor interface and the RAM is coupled to the memory interface

23. The integrated core logic of claim 22, wherein the integrated core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, a parallel interface, an input device interface, and a peripheral connect interface bus (PCI) interface.

24. The integrated core logic of claim 22, wherein the integrated core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, an input device interface, and a PCMCIA interface.

25. An integrated core logic circuit comprising:

a display controller; and

embedded memory coupled to the display controller, the embedded memory comprising N separate buffers.

26. The integrated core logic circuit of claim 25, wherein the N buffers comprising a frame buffer and a DSTN buffer.

27. The integrated core logic circuit of claim 26, wherein the integrated core logic circuit further comprises a direct memory access (DMA) controller.

28. The integrated core logic circuit of claim 27, wherein the integrated core logic circuit further comprises a central processor interface and a memory interface, wherein the central processor and the ROM are coupled to the central processor interface and the RAM is coupled to the memory interface

29. The integrated core logic of claim 28, wherein the integrated core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, a parallel

interface, an input device interface, and a peripheral connect interface bus (PCI) interface.

30. The integrated core logic of claim 28, wherein the core logic circuit further comprises a encoder-decoder (CODEC) interface, a serial interface, an input device interface, and a PCMCIA interface.

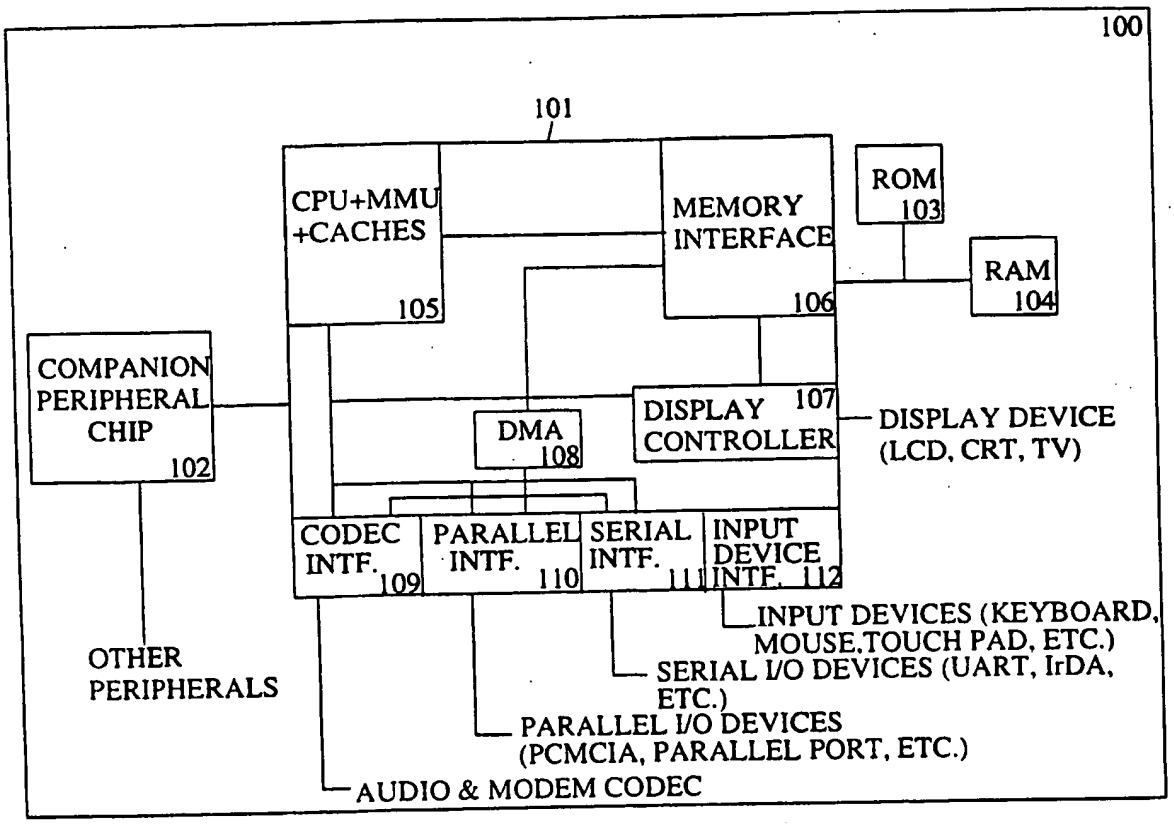

FIGURE 1
PRIOR ART

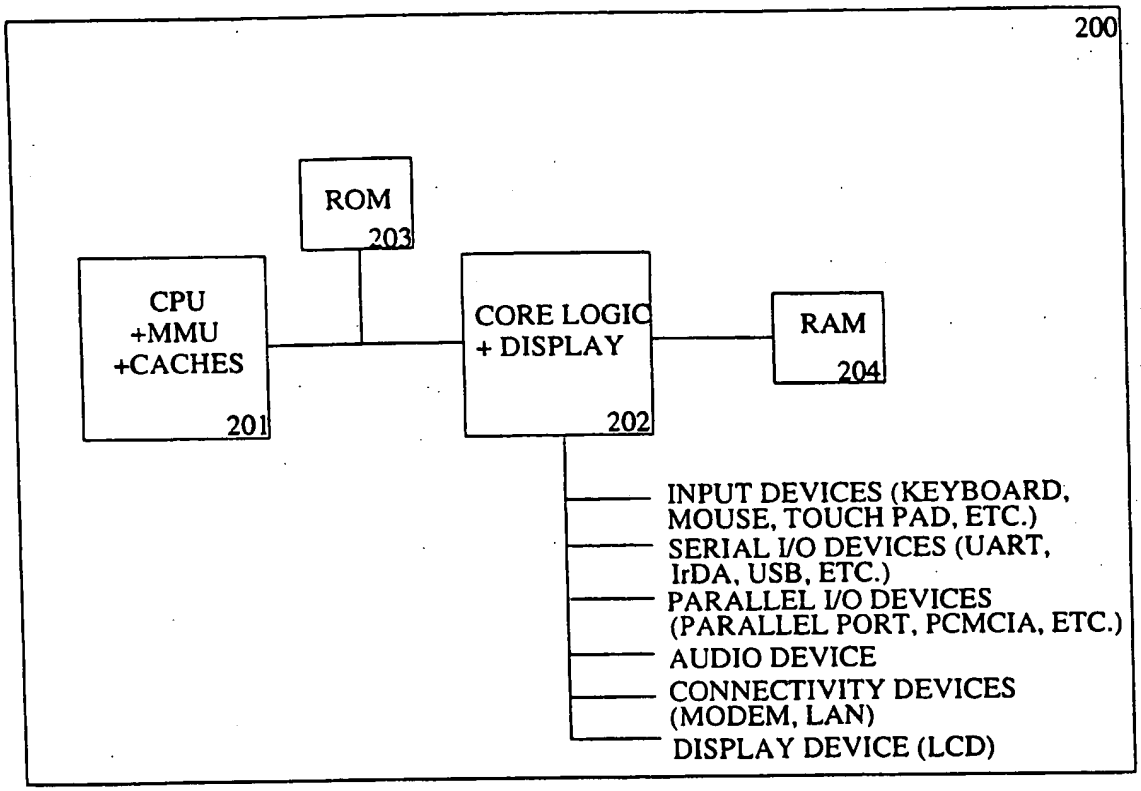

FIGURE 2
PRIOR ART

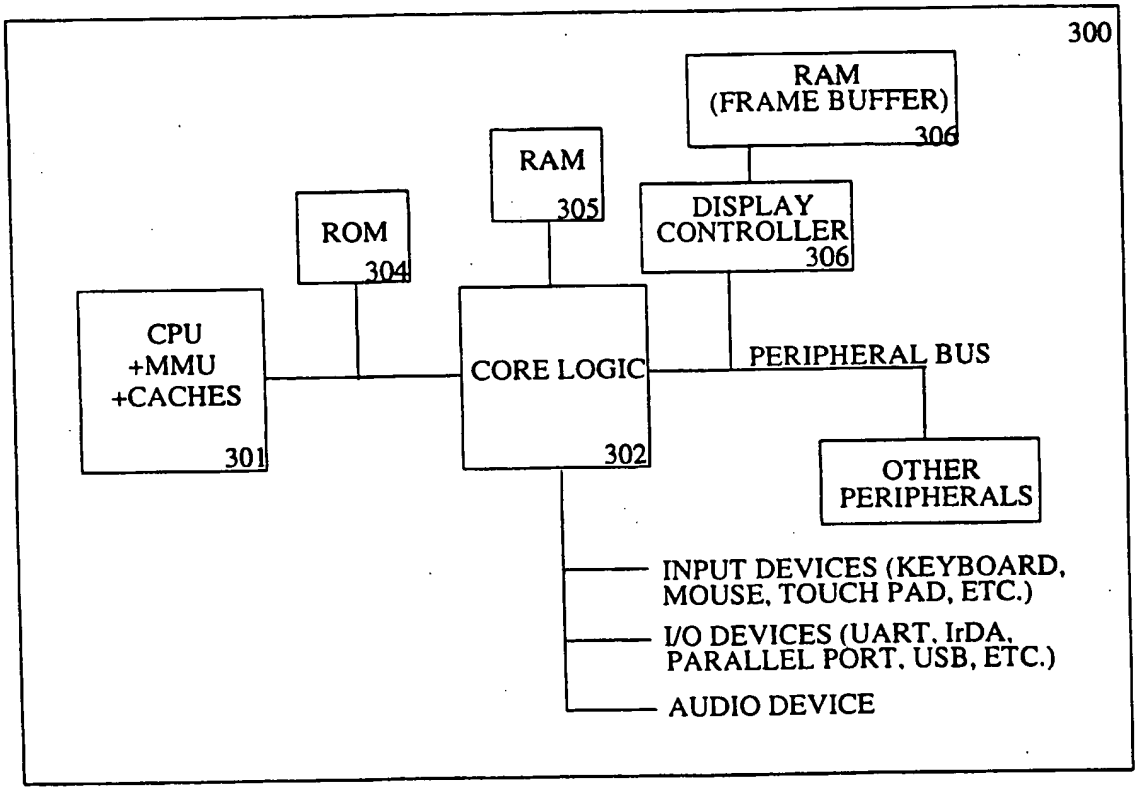

FIGURE 3
PRIOR ART

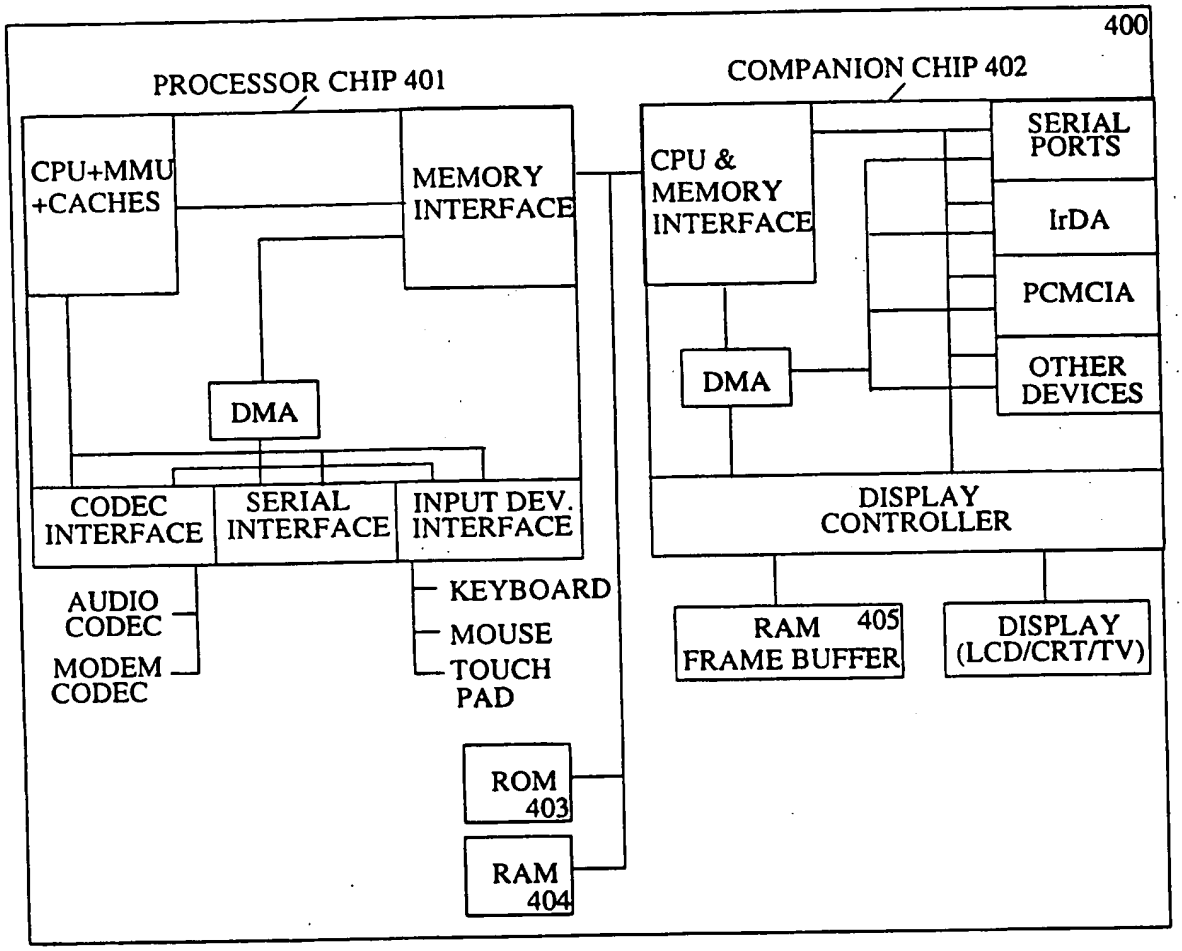

FIGURE 4
PRIOR ART

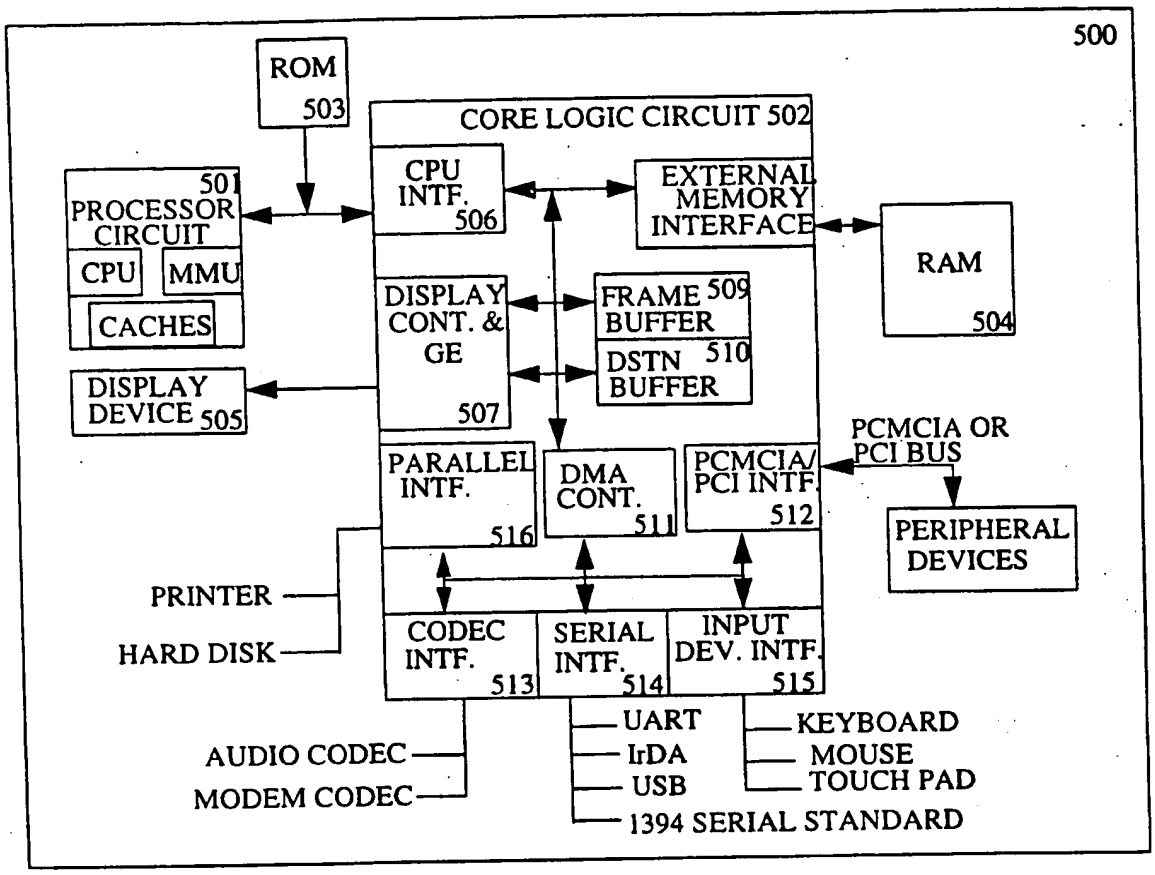
500
ROM
503
CORE LOGIC CIRCUIT 502
501
PROCESSOR CIRCUIT
CPU
MMU
CACHES
CPU INTF. 506
EXTERNAL MEMORY INTERFACE
RAM
504
DISPLAY CONT. & GE
507
FRAME BUFFER 509
DSTN BUFFER 510
DISPLAY DEVICE 505
PCMCIA OR PCI BUS
PARALLEL INTF. 516
DMA CONT. 511
PCMCIA/ PCI INTF. 512
PERIPHERAL DEVICES
PRINTER
HARD DISK
CODEC INTF. 513
SERIAL INTF. 514
INPUT DEV. INTF. 515
UART
IrDA
USB
1394 SERIAL STANDARD
KEYBOARD
MOUSE
TOUCH PAD
AUDIO CODEC
MODEM CODEC

FIGURE 5

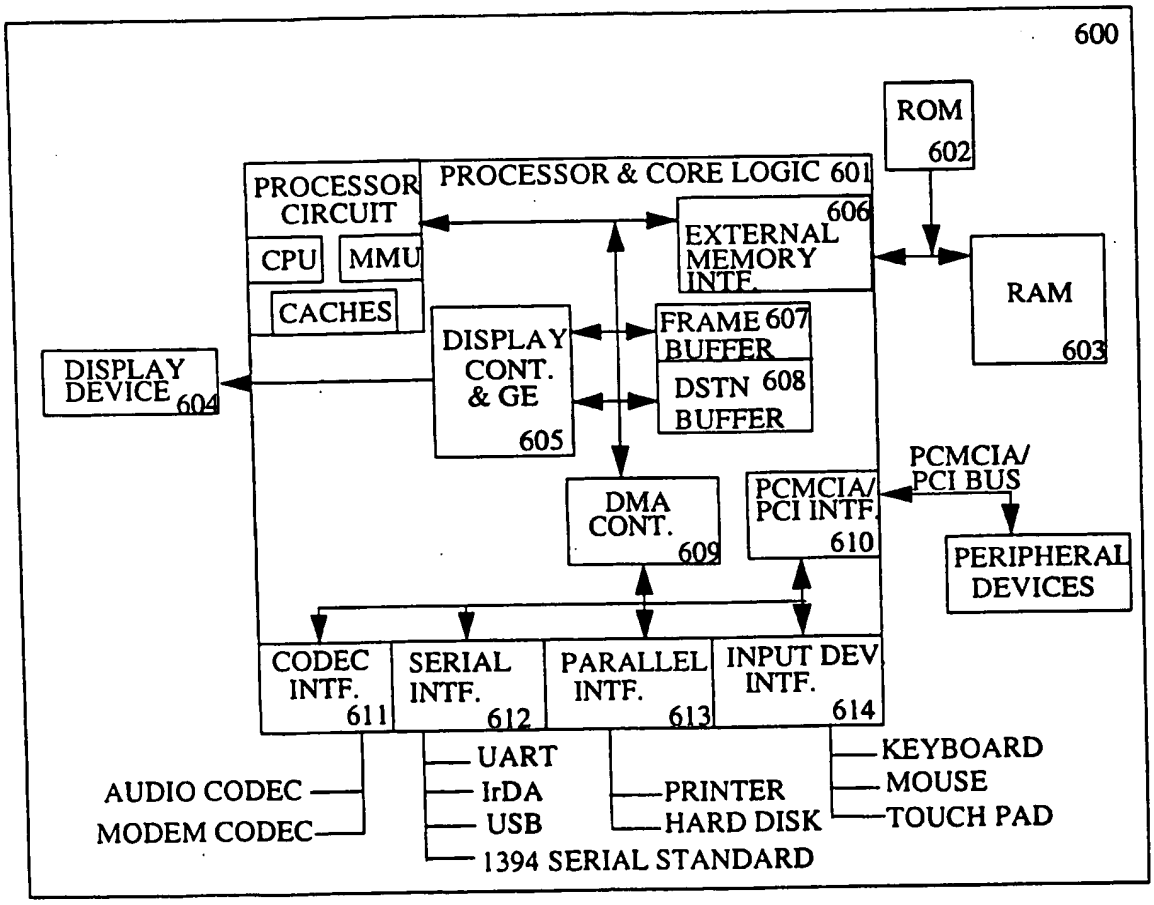
600
ROM
602
PROCESSOR CIRCUIT
PROCESSOR & CORE LOGIC 601
CPU
MMU
CACHES
606
EXTERNAL MEMORY INTF.
RAM
603
DISPLAY DEVICE 604
DISPLAY CONT. & GE
605
FRAME 607 BUFFER
DSTN 608 BUFFER
PCMCIA/ PCI BUS
DMA CONT.
609
PCMCIA/ PCI INTF.
610
PERIPHERAL DEVICES
CODEC INTF.
611
SERIAL INTF.
612
PARALLEL INTF.
613
INPUT DEV INTF.
614
AUDIO CODEC
MODEM CODEC
UART
IrDA
USB
1394 SERIAL STANDARD
PRINTER
HARD DISK
KEYBOARD
MOUSE
TOUCH PAD

FIGURE 6

INTERNATIONAL SEARCH REPORT

ernational Application No
PCT/US 98/25285

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G09G1/16 G06F15/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G09G G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 96 41325 A (S MOS SYSTEMS INC) 19 December 1996 see page 7, line 1 - page 8, line 21	1,2,10, 11,19,25
A	see page 10, line 12 - page 11, line 8; figures 4,5	3-6, 12-15, 20,21, 26,27

X	WO 97 06523 A (CIRRUS LOGIC INC) 20 February 1997	19-21, 25-27
A	see page 11, line 6 - page 17, line 24; figures 1,3	1-7, 10-16, 22,28

A	WO 97 26604 A (MONOLOTHIC SYSTEM TECHNOLOGY I) 24 July 1997	1-5, 10-14, 19,20,26
X	see the whole document	25

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 April 1999	26/04/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl. Fax: (+31-70) 340-3016	Michel, T

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INTERNATIONAL SEARCH REPORT

.ernational Application No
PCT/US 98/25285

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 691 745 A (MITAL AMIT) 25 November 1997 see the whole document	1-4, 10-13, 19,20, 25,26
A	FR 2 674 361 A (JAEGER) 25 September 1992 see the whole document	1-4, 10-14, 19,20, 25,26
A	BURSKY D: "486 CPU PACKS PERIPHERALS FOR REAL-TIME SYSTEM NEEDS" ELECTRONIC DESIGN, vol. 43, no. 18, 5 September 1995, page 167/168 XP000535289 see the whole document	1,6-10, 15-19, 21-25, 27-30

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

.ernational Application No
PCT/US 98/25285

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WO 9706523 A	20-02-1997	EP 0843872 A	27-05-1998
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US 5691745 A	25-11-1997	NONE	
FR 2674361 A	25-09-1992	NONE	